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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,607	07/01/2003	Yun-Sheng Chen	JCLA10931	4794

7590 03/29/2004

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EXAMINER	
SOWARD, IDA M	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 03/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/612,607	CHEN, YUN-SHENG	
	Examiner	Art Unit	
	Ida M Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) *1-8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9 and 10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the election filed February 27, 2004.

Election/Restrictions

Applicant's election without traverse of Group I, claims 9-10 in Paper No. 02-27-03 is acknowledged.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 2 recites the limitation "**the amorphous silicon layer**" on page 11, lines 21-22. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

> the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamada (5,888,856) in view of Miyasaka (6,124,154).

In regard to claim 9, Hamada teaches a low temperature poly-silicon thin film transistor (LTPS TFT), comprising: a poly-silicon layer 102, deposited on a substrate 101, and the poly-silicon layer comprises a source, a drain, and a channel that is deposited in between the source and the drain, a gate isolation layer, 103 deposited on the substrate, and covering the poly-silicon layer; a gate 104, correspondingly deposited on the gate isolation layer that is deposited above the channel; a dielectric layer 105, deposited on the gate isolation layer, and covering the gate; a source metal layer 106, deposited on a surface of the dielectric layer and in the dielectric layer and the gate isolation layer wherein the source metal layer is electrically connected to the source; and a drain metal layer 106, deposited on the surface of the dielectric layer and in the dielectric layer and the gate isolation layer wherein the drain metal layer is electrically connected to the drain (Figure 1, cols. 2-3, lines 50-67 and 1-55, respectively).

As best understood and in regard to claim 10, Hamada teaches a buffer layer 2 in between the substrate 1 and the amorphous layer 3a (Figures 4I-4J, cols. 3-5, lines 56-67, 1-67 and 1-25, respectively).

However, Hamada fails to teach a height/width ratio of a plurality of mounds on a surface of the poly-silicon layer is less than 0.2. In the specification of the claimed invention, having a height/width ratio of a plurality of mounds on a surface of the poly-silicon layer being less than 0.2 is not shown as being critical. Miyasaka teaches a

laser anneal treatment of a poly-silicon layer which improves film surface (cols. 16-17, lines 40-67 and 1-7, respectively).

Since Hamada and Miyasaka are from the same field of endeavor (low temperature poly-silicon thin film transistors), the purpose disclosed by Miyasaka would have been pertinent in the art of Hamada. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the low temperature poly-silicon thin film transistor as taught by Hamada with the low temperature poly-silicon thin film transistor having laser anneal treatment of the poly-silicon layer as taught by Miyasaka to provide high yield, high reliability thin film transistors (col. 3, lines 19-30).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to low temperature poly-silicon thin film transistors (LTPS TFTs):

Kubota et al. (US 6,300,927 B1) Matsueda (US 6,281,700 B1)

Ohtani et al. (6,011,275) Yamazaki (US 6,207,969 B1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M Soward whose telephone number is 571-272-

1845. The examiner can normally be reached on Monday - Thursday, 6:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
March 18, 2004

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800